What is claimed is:

1. A semiconductor device, comprising:

a first doping region, which has a first conduction type;

a second doping region, which has the first conduction type and is spaced apart from the first doping region;

a channel region, which lies between the first and second doping regions and has a second conduction type; and

a gate structure provided above the channel region, wherein

the gate structure having a first gate dielectric made of a first material with a first thickness and a first dielectric constant, which is situated directly above the channel region, and an overlying second gate dielectric made of a second material with a second thickness and a second dielectric constant, which is significantly greater than the first dielectric constant, and

the first thickness of the first gate dielectric and the second thickness of the second gate dielectric configured such that the corresponding thickness of a gate structure with the first gate dielectric, to obtain a same threshold voltage, is at least of a same magnitude as a thickness equal to a sum of the first thickness and the second thickness.

2. The semiconductor device according to claim 1, wherein the first material is silicon dioxide and the second material is a transition metal oxide.

3. The semiconductor device according to claim 2, wherein the second material is a binary metal oxide selected from the group of: Al_2O_3, Y_2O_3, La_2O_3, TiO_2, ZrO_2, HfO_2.

4. The semiconductor device according to claim 1, wherein the gate structure has a third gate dielectric (155) made of silicon dioxide, which is provided above the second gate dielectric (150).

5. The semiconductor device according to claim 1, wherein a field-effect transistor is involved.

6. The semiconductor device according to claim 1, wherein a parasitic field-effect transistor is involved.

7. The semiconductor device according to claim 6, wherein the first doping region is a filling electrode of a trench capacitor of a memory cell, the second doping region is a semiconductor substrate and the channel region is a connection region of an associated selection transistor to a gate connection of the filling electrode and the gate structure comprises an insulation collar of the trench capacitor.

8. The semiconductor device according to claim 7, wherein a trench capacitor dielectric made of the second gate dielectric is provided below the insulation collar.

9. The semiconductor device according to claim 6, wherein the first doping region and the second doping region are provided at a surface of a semiconductor substrate and are isolated by an isolation trench filled with an insulator material, and the gate structure is provided at least on the trench bottom.

10. The semiconductor device according to claim 9, wherein the gate structure is provided on the trench bottom and the trench walls.

11. The semiconductor device according to claim 9, wherein the isolation trench has a greater depth extent in the semiconductor substrate than the first doping region and the second doping region.

12. A method for fabricating a semiconductor device to form a gate structure, comprising:

providing a first gate dielectric made of silicon dioxide directly above a channel region; and

providing an overlying second gate dielectric made of binary metal oxide.

13. A method for fabricating a semiconductor device to form a gate structure, comprising:

providing a first gate dielectric made of a binary metal oxide directly above a channel region; and

providing a second gate dielectric made of silicon dioxide below the first gate dielectric by means of a thermal annealing process in an oxygen-containing atmosphere.

14. A method for fabricating a semiconductor device, having a trench capacitor dielectric made of a second gate dielectric provided below an insulation collar, to form the gate structure, comprising:

providing a first gate dielectric made of binary metal oxide on a surface of a trench for the trench capacitor;

providing a filling electrode in the lower trench region; and

providing a second gate dielectric made of silicon dioxide below the first gate dielectric by means of a thermal annealing process in an oxygen-containing atmosphere in an upper trench region;

forming an insulation collar and a buried connection in the upper trench region.